

Wideband CMOS Integrated RF Combiner for LINC Transmitters

Sotoudeh Hamed-Hagh, C. André T. Salama

Edward S. Rogers Sr. Department of Electrical and Computer Engineering

University of Toronto

10 King's College Road, Toronto, Ontario, M5S 3G4, Canada

Tel: (416) 978-8658, Fax: (416) 978-4516

Email: salama@vrg.utoronto.ca

Abstract - The design of a novel wideband RF signal combiner suitable for LINC transmitters in CMOS technologies is presented in this paper. Compared to the conventional narrowband design, the wideband architecture achieves a small reflection coefficient (less than 0.3) suitable for wideband spread spectrum multi-user mobile systems. A 0.18 μ m CMOS wideband signal combiner, designed to add two 8GHz signals and deliver 1.5W to the antenna from 1V class F power amplifiers, is presented and compared to a narrowband design.

I. INTRODUCTION

To achieve a high capacity and bandwidth efficiency in cellular networks, future generations of mobile handsets will utilize channelizations like WCDMA and modulations like QPSK. As a result, the transmitter must be extremely linear to preserve the narrowbandness of the output signal. The Power Amplifiers (PAs) at the output of the transmitter must provide the linearity required by the communication scheme at the maximum output power to avoid any distortion of the envelope of the signal. This linearity must be maintained over a large bandwidth required by the high channel bit-rates at radio frequencies. The PAs must also exhibit high efficiency to be suitable for use in portable devices, where battery size and life are at a premium.

Designing a linear transmitter architecture for spectrally efficient communication systems, using constant envelope signals in conjunction with nonlinear PAs, can result in excellent power efficiency. To achieve this objective, systems like LINC (Linear amplification using Nonlinear Components) [1], CALLUM (Combined Analog Locked Loop Universal Modulator) [2] and VLL (Vector Locked Loop) [3] have been developed.

The essence of the LINC transmitter realization, illustrated in Fig. 1, is to represent an envelope varying signal by two constant envelope signals with varying phases and amplify them separately using nonlinear amplifiers. The two signals are given by

$$s_1(t) = r_{\max} e^{j[\omega_c t + \phi(t) + \theta(t)]} \quad (1)$$

$$s_2(t) = r_{\max} e^{j[\omega_c t + \phi(t) - \theta(t)]} \quad (2)$$

where $\phi(t)$ is given by

$$\phi(t) = \tan^{-1} \left[\frac{s_q(t)}{s_i(t)} \right] \quad (3)$$

and $\theta(t)$ is given by

$$\theta(t) = \cos^{-1} \left[\frac{\sqrt{s_i^2(t) + s_q^2(t)}}{2r_{\max}} \right] \quad (4)$$

$s_i(t)$ and $s_q(t)$ are quadrature baseband signals and r_{\max} is the maximum peak of the envelope. The two amplified constant envelope, varying phase signals are then added together to produce an amplified linear replica of the input signal.

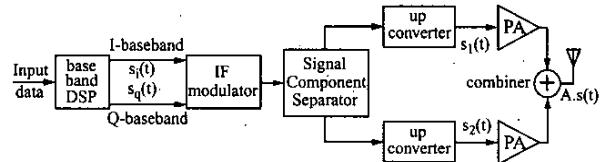


Fig. 1. The LINC transmitter front-end

One of the main bottlenecks in the design of a LINC transmitter is how to combine the two wideband constant envelope signals on-chip with minimum loss. Using active combiners is not possible because of high loss and nonlinearity introduced at high output power levels specially at high frequencies. Using passive combiners which feature wideband low loss characteristics are therefore the preferred alternative.

The design of a CMOS wideband RF signal combiner suitable for LINC transmitters and its performance compared to a conventional narrowband design are presented in this paper.

II. CIRCUIT DESIGN

The power amplifiers of the LINC transmitter can be realized using one of the nonlinear switching architectures such as class E or class F. A class E PA, can achieve maximum efficiency at low supply voltages because of its higher optimum load compared to a class F design [4]. However, a class E PA requires the power switch to handle higher voltages as compared to a class F design making the class F the preferred alternative to realize the PAs.

A possible realization of the LINC transmitter front-end using class F PAs is illustrated in Fig. 2. The quarter wavelength ($\lambda_0/4$) transmission lines connected between the

switching transistors and the antenna perform three tasks. First, they form the class F PA architectures [5, 6], second, they make the summation of the two constant envelope with varying phase signals feasible at the antenna [7] and third, they match the output resistance of the switching transistors to the antenna through the transformation

$$Z_{in} = \frac{Z_0^2}{Z_{out}} \quad (5)$$

where Z_0 is the characteristic impedance of the $\lambda_0/4$ transmission lines, Z_{in} is the effective impedance at the drain of the power transistors and Z_{out} is the impedance of the antenna.

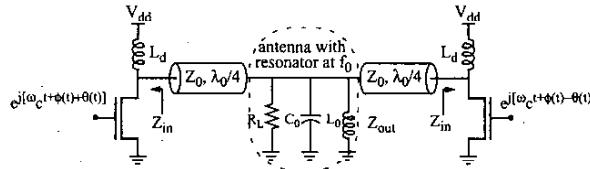


Fig. 2. Realization of the LINC transmitter front-end

Realizing the LINC transmitter front-end using off-chip $\lambda_0/4$ transmission lines achieves the best performance but results in a bulky design. Using on-chip $\lambda_0/4$ transmission lines occupies a large silicon area and results in a costly design. Realizing on-chip $\lambda_0/4$ transmission lines with lumped elements is a possible alternative to achieve an economical and compact design. The realization of such lumped transmission lines and their wideband matching characteristics are discussed in the following section.

A. Realizing On-Chip $\lambda_0/4$ Transmission Lines with Lumped Elements

Cascades of n segments of LC ladder low pass networks can be designed to emulate the delay characteristics of a $\lambda_0/4$ transmission line as shown in Fig. 3.

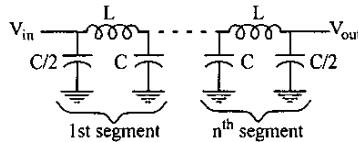


Fig. 3. A LC ladder network to realize lumped transmission line

The values of L and C in the Π configuration must be selected as follows [7]

$$L = \frac{Z_0}{4nf_0} \quad (6)$$

and

$$C = \frac{1}{4nf_0 Z_0} \quad (7)$$

where f_0 is the operating frequency of interest and n is the number of Π segments used to realize the $\lambda_0/4$ LC ladder network. The cutoff frequency of the lumped line is given by [8]

$$f_c = \frac{1}{\pi\sqrt{LC}} \quad (8)$$

Emulating the transmission lines with a large number of lumped on-chip inductors and capacitors [7], increases the cutoff frequency of the lumped line, but results in large signal loss and reduced efficiency because of the long signal path from the PAs to the antenna. The loss is due to the substrate coupling, high sheet resistance and high frequency skin effect of the metal layers used in modern IC technologies.

B. Wideband Impedance Matching

Impedance matching using a single $\lambda_0/4$ line, as illustrated in Fig. 4(a), uses one step to transform Z_{in} to Z_{out} . For large impedance transformation ratios, the reflection coefficient between the two impedances increases resulting in a narrowband impedance transformation.

To achieve wideband impedance matching, the transformation must be performed in smaller ratios to reduce the reflection coefficients between the transformed impedances. The Impedance matching using cascades of three lines is illustrated in Fig. 4(b).

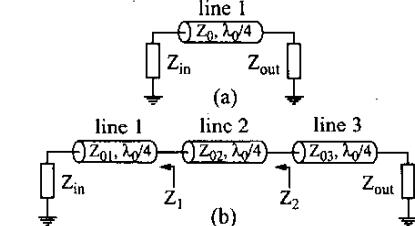


Fig. 4. Impedance matching using, (a)single line, (b)cascades of three lines

In this case, the impedance Z_1 and Z_2 looking into the outputs of lines 1 and 2 respectively must satisfy

$$Z_{in} < Z_1 < Z_2 < Z_{out} \quad (9)$$

As a result, the characteristic impedances Z_{01} , Z_{02} and Z_{03} of the cascaded lines must satisfy the equation

$$Z_{01} < Z_{02} < Z_{03} \quad (10)$$

Since the impedance matching in the two approaches illustrated in Fig. 4 aim to achieve the same overall transformation ratio from Z_{in} to Z_{out} , therefore

$$Z_0 = \frac{Z_{01} \cdot Z_{03}}{Z_{02}} \quad (11)$$

Therefore, equation(10), implies that

$$Z_{01} < Z_0 < Z_{03} \quad (12)$$

and from equation(7), it results that the lumped capacitance required to realize Z_{01} is larger than the one needed to realize Z_0 . To deliver a large output power to the antenna, a large power transistor with high current handling capability is required. Such a transistor has a large parasitic capacitance at its drain which can be included in the realization of Z_{01} .

III. EXPERIMENTAL RESULTS

The 8GHz narrowband and wideband $\lambda_0/4$ lumped line combiners use the two top metal layers (35 μ m wide) in a 0.18 μ m CMOS technology, to realize low loss signal paths and

inductors. The inductors were optimized and characterized using Momentum simulator of HPADS. The circuits and chip micrographs of the narrowband and wideband $\lambda_0/4$ combiners are shown in Figs. 5 and 6 respectively, and are designed to transform 0.55Ω impedance to match the 50Ω antenna.

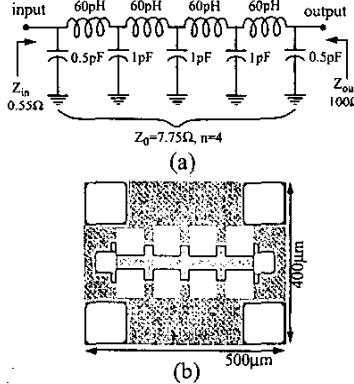


Fig. 5. Narrowband $\lambda_0/4$ lumped line, (a) schematic, (b) chip micrograph

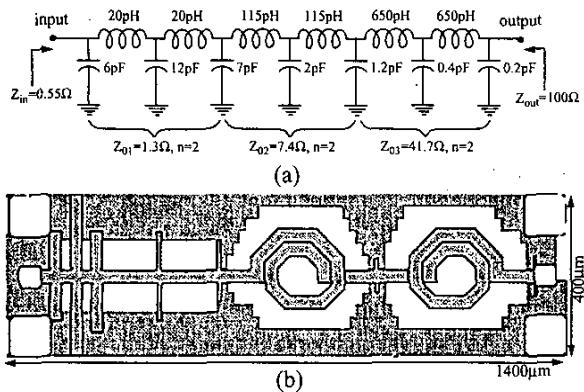


Fig. 6. Wideband $\lambda_0/4$ lumped line, (a) schematic, (b) chip micrograph

Small inductors were realized using metal strips. The large 650pH inductors were realized using 1.5 turns octagonal shape layout with $120\mu\text{m}$ outer radius and $0.6\mu\text{m}$ spacing. The strip inductors were modeled using a series combination of resistance and inductance while for 650pH inductor, the Π model shown in Fig. 7 was used.

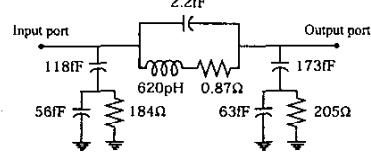


Fig. 7. Equivalent Π model of the 650pH inductors

The measured S-parameters of the two $\lambda_0/4$ combiners, shown in Figs. 8 and 9, were obtained from 130MHz up to 20GHz using a HP8720B Vector Network Analyzer with 100Hz IF bandwidth. No on-chip output resonator was used to suppress harmonics other than the 8GHz frequency. The input and output reflection coefficients (GAMMA) of the

narrowband and wideband $\lambda_0/4$ lumped lines, are shown in Figs. 10 and 11. For the narrowband $\lambda_0/4$ combiner, the input and output S-parameters and reflection coefficients are the same because of the design symmetry.

In general, the relative inaccuracy of the simulation results compared to the measurement is due to the modeling imperfections of the small strip inductors. Comparing the GAMMA of the wideband and narrowband $\lambda_0/4$ combiners shows that the input and output reflection coefficients of the wideband design are smaller than those of the narrowband design over a wider bandwidth centered at 8GHz frequency. As a result, the wideband design can achieve better matching and improved efficiency for broadband communications.

IV. CONCLUSION

The design of a wideband RF signal combiner suitable for LINC transmitters in CMOS technologies was presented in this paper. Compared to the conventional narrowband combiner design using a single quarter wavelength lumped line, the wideband architecture results in a small reflection coefficient, (0.3), over a large bandwidth making it suitable for spread spectrum multi-user mobile systems. The narrowband and wideband $\lambda_0/4$ lumped lines were designed in a standard $0.18\mu\text{m}$ CMOS to add two 8GHz signals and to match 0.55Ω source resistance to a 50Ω antenna and deliver 1.5W power from a 1V supply class F power amplifier. The narrowband and wideband $\lambda_0/4$ lumped lines occupy an area of $400\times 500\mu\text{m}^2$ and $400\times 1400\mu\text{m}^2$ respectively.

ACKNOWLEDGEMENTS

The authors acknowledge the financial support of NSERC, Micronet, Gennum, Nortel Networks, PMC Sierra and Zarlink. The fabrication was carried out through the Canadian Microelectronics Corporation.

REFERENCES

- [1] D. C. Cox, "Linear Amplification with nonlinear components," *IEEE Trans. on Communication*, vol.COM-22, pp.1942-1945, 1974.
- [2] A. Bateman, "The Combined Analogue Locked Loop Universal Modulator (CALLUM)," *42nd IEEE Vehicular Technology Conference Proceeding*, pp.759-764, 1992.
- [3] M. K. DaSilva, "Vector Locked Loop", U.S. Patent 5105168, Apr. 14, 1992.
- [4] T. Sowlati, C.A.T. Salama, J. Sitch, G. Rabjohn and D. Smith, "Low voltage, high efficiency GaAs class E power amplifiers for wireless transmitters," *IEEE J. of Solid-State Circuits*, vol.30, pp.1074-1080, 1995.
- [5] F. H. Raab, "An introduction to Class F Power Amplifiers," *RF Design*, Vol.19, No.5, pp.79-84, 1996.
- [6] F. H. Raab, "Class-F Power Amplifiers with Maximally Flat Waveforms," *IEEE Trans. on Microwave Theory and Techniques*, Vol.45, No.11, pp.2007-2012, 1997.
- [7] A. Shirvani, D. K. Su, and B. A. Wooley, "A CMOS RF Power Amplifier with Parallel Amplification for Efficient Power Control," *IEEE J. of Solid-State Circuits*, Vol.37, No.6, pp.684-693, 2002.
- [8] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Cambridge University Press, Cambridge, 1998.

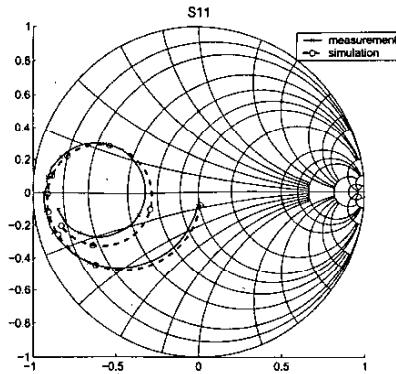


Fig. 8. The S-parameters of the narrowband $\lambda_0/4$ lumped line combiner for input and output ports

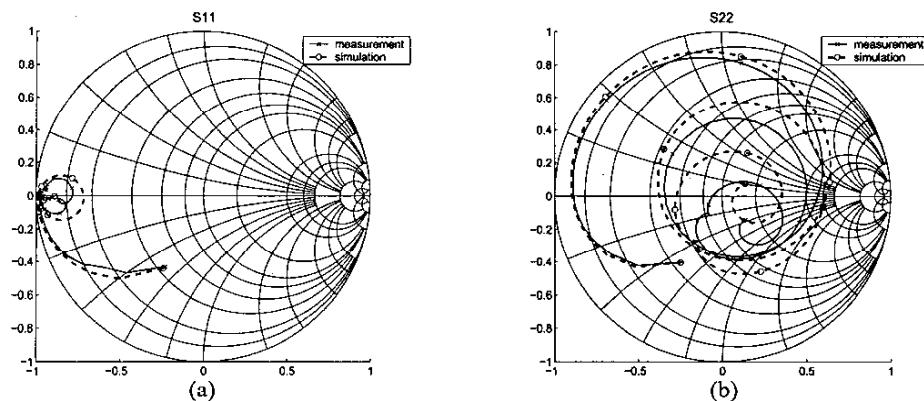


Fig. 9. The S-parameters of the wideband $\lambda_0/4$ lumped line combiner, (a) input port, (b) output port

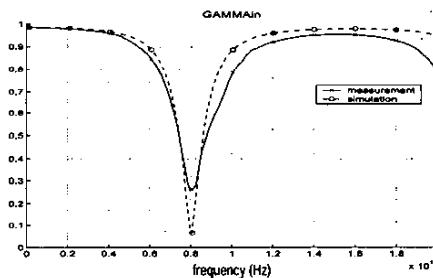


Fig. 10. The reflection coefficient of the narrowband $\lambda_0/4$ lumped line combiner for input and output ports

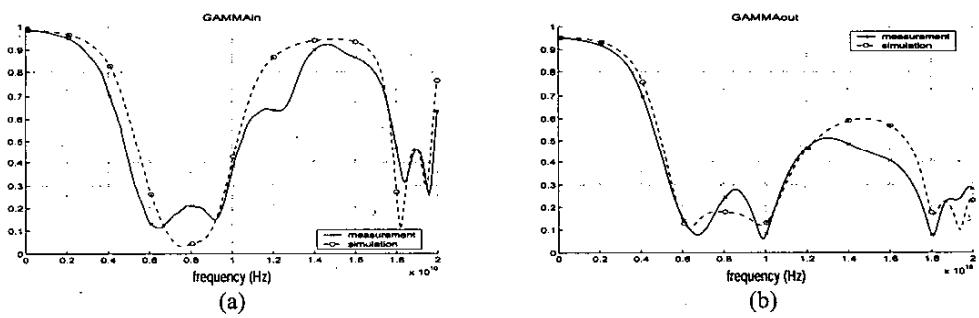


Fig. 11. The reflection coefficient of the wideband $\lambda_0/4$ lumped line combiner, (a) input port, (b) output port